IN THE SPECIFICATION:

Please amend page 1, last paragraph and the subsequent paragraphs (continuing to page 2) as follows:

As the performance of accessing to this cache memory significantly affects the processing performance in the information processing apparatus, several schemes have been employed for expanding the bus width of the cache memory within the disk control device and/or for accelerating bus clocks to thereby further enhance the access performance to the cache memory. Additionally in JP-A-2000-250712, there is disclosed a method for providing a data transfer integrated circuit (selector) and for selecting, when contention or conflict occurs between access requests ~~with respect~~ to a cache memory, a certain number of ones from among the access requests, which number corresponds to the number of data buses coupled to the cache memory.

Unfortunately, since there is a limitation of the space in the substrate which can be utilized for the disk array device, it is difficult to expand the bus width of cache memory ~~currently available disk array devices are faced with a limit in size of a substrate used, which in turn leads to difficulties in further expansion of the bus width of cache memory~~.

SUMMARY OF THE INVENTION

In the method as disclosed in JP-A-2000-250712, a time required for data transfer becomes shorter due to expanding of data bus width ~~expansion or the like,~~ so that an overhead for data bus allocation control causes deterioration of utilization efficiency of the data bus ~~serves to lower the use efficiency of data buses~~.

Accordingly, a need is felt to reduce the ~~ratio of a~~ time necessary for control processes in ~~taken to provide controls within~~ the data transfer integrated circuit among the time of ~~which occupies~~ an entire data transfer operation without having to expand the bus width of the cache memory, to thereby improve an effective speed relative to accessing to the cache memory.

Please amend page 2, last paragraph (continuing to page 3) as follows:

A disk array device in accordance with one aspect of the present invention which attains the foregoing object includes a plurality of channel control units for performing data transfer and reception between these units and an information processing apparatus that is communicably connected thereto, a plurality of disk control units for performing data transfer and reception between these units and a plurality of hard disk drives as communicably connected thereto, a CPU for performing control of the plurality of channel control units and the plurality of disk control units, a cache memory for storage of data being transferred and received between the channel control units and the disk control units, and a data transfer integrated circuit which is communicably connected via one or more ~~than one~~ buses to the channel control units, the disk control units and the CPU and also connected via a plurality of data buses to the cache memory, wherein when receiving a request for access to the cache memory from any one of the channel control units, the disk control units and the CPU, the data transfer integrated circuit accesses to the cache memory by using ~~more than one of~~ the data buses, a number of which is determined in accordance with a transfer data length that is set in the access request.